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A DIGITAL FREQUENCY SYNTHESIZER-DIVIDER USING A PHASE LOCK LOOP--ETC(U)
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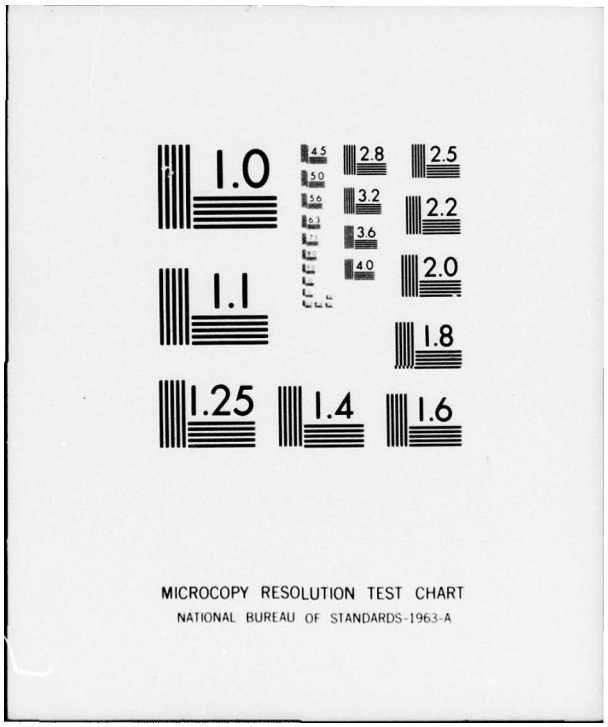
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ROYAL AIRCRAFT ESTABLISHMENT

A DIGITAL FREQUENCY SYNTHESIZER-DIVIDER USING A PHASE LOCK LOOP CONTROL SYSTEM

by

J. Lillie

October 1976

(14) RAE-TM-Rad-Nav-43

ROYAL AIRCRAFT ESTABLISHMENT

(9) Technical Memorandum Rad-Nav 43

Received for printing 26 October 1976

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(18) DRIC

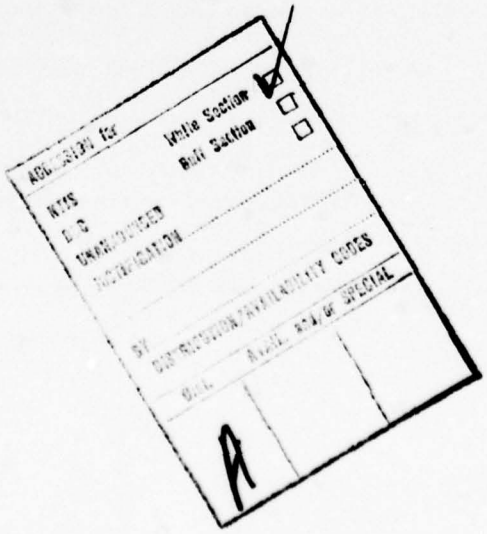
(19) BR-54979

(11) Oct 76

(12) 24p.

SUMMARY

The design of a digital frequency synthesizer-divider using a phase lock loop control system is described. The device is for laboratory use as a programmable frequency source having a stable output.



CONTENTS

1 INTRODUCTION

The aim of this project was to design and construct a frequency synthesizer-divider covering the range 10Hz to 1MHz and variable in 10, 100 or 1000Hz steps. Such an equipment would be used in the laboratory as a stable but variable square wave generator for testing digital circuits.

There are many frequency generator circuits but the most popular is that which uses phase locked loop, PLL techniques. Using a PLL method enables a large range of frequencies to be produced with the output having good frequency resolution and high stability. The signal generator-frequency synthesizer design undertaken was based on the use of a micropower PLL integrated circuit.

The frequency synthesizer-divider described in this Memorandum was designed and constructed as a student summer vacation project.

2 PHASE LOCK LOOP OPERATION

The basic components of a phase lock loop, see Fig.1, are a phase comparator, a low pass filter and a voltage controlled oscillator, VCO. In the phase comparator the frequencies and phases of the input signal, V_I , and the VCO output, V_0 , are compared and an error voltage, V_d , proportional to the differences, is produced. The error voltage is filtered by the low pass filter and then applied to the control element of the VCO. The VCO control voltage, V_c , changes the frequency and phase of the output in such a way that the frequency and phase difference between the output, V_o , and input V_I , signal is reduced. When the VCO frequency is sufficiently close to the input frequency, the closed-loop nature of the PLL forces the VCO to lock in frequency with the signal input, i.e. when the PLL is in lock, the VCO frequency is identical to the signal input.

The filtering of the error voltage, V_d , is required in order to smooth out the high frequency components. It also attenuates any fast changes that occur in the error voltage due to the noise in the input signal.

The phase comparator is basically a multiplier, so for sinusoidal waveforms, $V_I = V \cos(\omega_1 t + \phi_1)$, $V_0 = V \cos(\omega_0 t + \phi_0)$ as inputs, an output signal, $V_d = V/2 \cos((\omega_1 + \omega_0)t + \phi_1 + \phi_0) + V/2 \cos((\omega_1 - \omega_0)t + (\phi_1 - \phi_0))$ is produced. The higher frequency component is removed by the low pass filter so that the VCO control voltage, V_c , consists of a signal that is constant when $\omega_1 = \omega_0$, i.e. when the input and output frequencies are identical the VCO control voltage is constant.

With no inputs to the phase comparator, the VCO operates at its free-running frequency. The PLL's capture range, $2f_c$, is defined as the range of frequencies about f_0 over which the loop will acquire lock with an input signal initially starting out of lock. The lock, or tracking, range, $2f_L$, of the PLL is defined as the range of frequencies about f_0 over which the VCO, once locked to the input signal, will remain locked.

Using the PLL for frequency synthesis a divide-by-N counter is placed in the feedback loop (see Fig.2). The operation of the loop is the same in that the VCO is adjusted until the two inputs to the phase comparator are equal in frequency and phase. The difference is that for the inputs to be identical, the frequency of the VCO must be N times greater than the input frequency. This is because it is divided down by N before the comparison of signals occurs. So we have an output whose frequency is N times as great as the input signal. If the divide-by-N counter is programmable then the output frequency can be altered by changing the value of N. If an input signal of 1kHz was used and N set at 1023 the output frequency will be 1.023MHz, thus high frequencies having low resolution can be achieved.

3 DESIGN

3.1 Basic layout

The basic system used is comprised of three main sections, a reference frequency generator, a programmable divide-by-N counter and a PLL.

The circuitry was designed so that the programmable divide-by-N counter could be switched between (a) being used in conjunction with the PLL for frequency synthesis, or (b) being used by itself to give an output that is a reference frequency divided down by N. The block diagram for the basic layout is shown in Fig.3.

It was decided to provide reference signals having frequencies of 1MHz, 100kHz and 10kHz for the divide mode and 1kHz, 100Hz and 10Hz for the synthesis mode. The choice of which mode the circuit operated in and which reference frequency was used was performed by analogue switching controlled by front panel mounted switches. Provision was also included whereby the circuit could operate from an externally applied reference source.

3.2 Reference frequency generator

The accuracy of the frequency sunthesizer is based on a 3MHz crystal controlled oscillator that serves as a stable frequency source for the derivation

of the various reference frequencies. The oscillator circuit was built using a COS-MOS NOR gate. The circuit comprises one NOR gate with all its inputs tied together and a 3MHz crystal, a 20MΩ resistor and a 3-15pF variable capacitor in parallel, connected between the gates input and output. The variable capacitor enabled the oscillator frequency to be adjusted. The crystal was housed in a miniature crystal oven to reduce frequency drift due to room temperature variations.

The 3MHz signal from the oscillator is then applied to a divider chain. The divider chain consists of a divide-by-three followed by five divide-by-ten stages. The divider chain was built using TTL integrated circuits but COS-MOS integrated circuits could have been used instead.

The divide-by-three stage is produced by using two JK flip-flops. The circuit is shown in Fig.4 along with the oscillator and divide-by-ten stages. The divide-by-ten stages are decade counters, a single IC being used for each. The reference frequencies available from the divider chain are 1MHz, 100KHz, 10kHz, 1kHz, 100Hz and 10Hz.

The output from the crystal oscillator is 10 volts peak-to-peak, therefore a voltage converter was required to make it TTL compatible at the divider chain input. A COS-MOS hex buffer-converter was used.

3.3 Programmable divide-by-N counter

A COS-MOS synchronous programmable divide-by-N counter, having a programmable range of 3 to 15999, was used for ease of compatibility with the PLL.

For operation in the synthesizer-divider the IC was set to operate as a four decade counter by means of three mode select inputs, thus giving a divide range of 3 to 9999. The decade counters are preset by means of sixteen 'jam' inputs[5] and the 'jam' inputs are set using four BCD thumbwheel switches. Each thumbwheel switch controls one decade of the counter. The counter detects when the programmed number, N , pulses has been counted and outputs a pulse of width $1/f_{IN}$ seconds.

3.4 Phase locked loop

A micropower phase locked loop was used. This PLL was chosen mainly because of its very low power consumption, typically 200mW. It is a digital IC and has an operating frequency range of up to 1.2MHz.

3.4.1 Phase comparator

There are two types of phase comparator in the IC. Phase comparator I is an exclusive OR network and requires input signals with a 50% duty cycle to maximize the lock range. This comparator, for frequency synthesis use, suffers from the disadvantage that it may lock onto input signals that are close to harmonics of the VCO centre frequency. Phase comparator II is an edge controlled digital memory network; this type of comparator acts only on the positive edges of the input waveforms hence the duty cycles of these waveforms are unimportant and has the further advantage of not locking onto harmonics of the input signal frequency. For these reasons phase comparator II was used.

Phase comparator II also supplies an output to show when the loop is locked. This is the phase pulses output, pin 1, and was used to drive a lock indicator circuit (see Fig.6).

3.4.2 Voltage controlled oscillator

To set the oscillator to a required frequency range one external capacitor, C_T , and one, or two, external resistors, R_T or R_T and R_0 , are required. Resistor, R_T , and capacitor, C_T , determine the maximum frequency range and resistor, R_0 , enables a frequency offset to be applied to the frequency range. Using the PLL for frequency synthesis we require full maximum frequency range possible. This means no offset is required, so resistor R_0 is omitted. The values of C_T and R_T to give the maximum frequency range are obtained from the COS-MOS data book[4].

3.4.3 Low pass filter

The low pass filter has to be externally provided to the IC. There are several low pass filter circuits but only two were tried in the design. These were simple RC filters, one being a simple lag filter and the other a two pole lag-lead filter. The two pole lag-lead filter should enable faster locking for step changes in frequency. It did prove to be the better of the two filters enabling the lower reference frequencies to be used.

The value of the lag-lead filter capacitor, C , required to give a satisfactory output was found experimentally to be very much larger than that recommended by the data book[4]. Increasing C to 10μF significantly reduced the level of jitter and the operation of the PLL was considered to be satisfactory.

3.5 Selection switching

The choice of the mode of operation of the synthesizer-divider and which reference frequency is used is by means of multiplexers-demultiplexers. For the reference frequency selection a COS-MOS dual differential four channel multiplexer was used (see Fig.5). A COS-MOS triple two channel multiplexer-demultiplexer was used for the mode of operation selection and also the output signal selection (see Fig.6).

The multiplexer-demultiplexer's control inputs are set by means of front panel mounted switches.

3.6 DIVIDE MODE OUTPUT SIGNAL SYMMETRY

The programmable divide-by-N counter is used by itself when the circuit is in the divide mode. The output from the counter consists of narrow pulses, it was decided that the output would be more useful if it had a 50% duty cycle. This was achieved by doubling the frequency of the counter input signal and then use a flip-flop at the output to divide by two to give a signal having a 50% duty cycle.

The frequency doubler consists of two monostables, that are operated so that they trigger on alternate edges of the reference signal, and have their outputs gated together by a NAND gate (see Fig.6). The monostables have to have pulse widths of less than half the lowest time period of the highest reference frequency 0.5μs, otherwise the pulses produced by each monostable would overlap producing an output that is permanently high (5 volts).

3.7 Interfaces

As both COS-MOS and TTL ICs are used in the design, voltage conversion to make signals compatible with other sections of the synthesizer-divider were required. To convert the TTL level (5 volts peak-to-peak) reference frequency outputs to compatible COS-MOS signals (10 volts peak-to-peak) for use by the PLL and the programmable divide-by-N counter a simple transistor circuit was used (see Fig.5). The design of the transistor interface is given in the Appendix. The output signal was of COS-MOS level and was converted to TTL level by means of a COS-MOS hex buffer-converter and also buffered using an SN7440 to give an output capable of driving thirty TTL gates.

4 POWER SUPPLY

The synthesizer-divider operates from +5 and +10 volts power supplies and the current consumption was found to be 220mA for the +5 volts and 380mA for the

+10 volts supplies, respectively. To avoid the necessity for two separate supplies a single 10 volt, 1A, supply was used, with the +5 volts being derived from it using an LM309K, 5 volt regulator. The supply wiring is shown in Fig.8.

5 CONSTRUCTION

All sub-assemblies were built on 'Veroboard', most of the unused copper track being removed to prevent distortion of the signal by capacitive coupling.

It was found that to obtain the greatest frequency range of the VCO, the timing capacitor, C_T , should be connected directly to the pins of the integrated circuit, also the copper track had to be removed from around these pins to prevent extra capacitance being added to the timing circuit.

6 PERFORMANCE

The output frequency range of the synthesizer-divider is given in Table 3. After a warm up time of five minutes the output was found to have an accuracy of 0.0001%.

Reference frequency	Output frequency (Hz)		Resolution	Mode
	Maximum	Minimum		
1kHz	1 000 000	3000	1kHz	Multiply
100Hz	999 900	300	100Hz	Multiply
10Hz	99 990	30	10Hz	Multiply
1MHz	333 333	100	-	Divide
100kHz	33 333	10	-	Divide
10kHz	3 333	1	-	Divide

When in the synthesis mode the output signal was found to have phase jitter particularly when the 10Hz reference frequency and a low value of N were selected but the output was considered satisfactory.

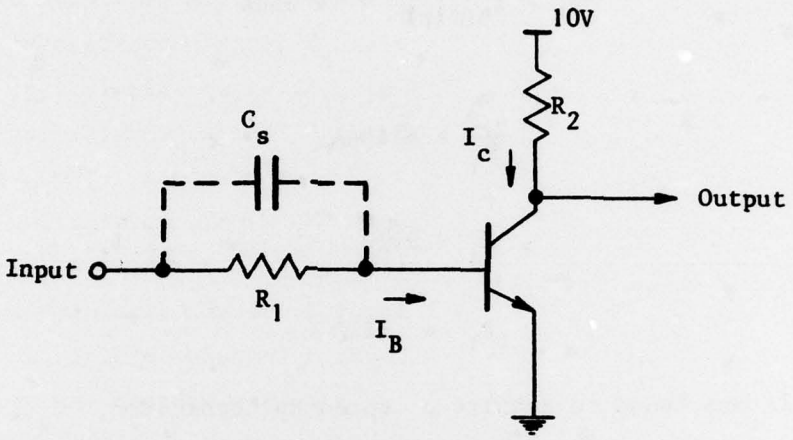
7 CONCLUSIONS

The PLL digital frequency synthesizer-divider built was found to comply with the requirements placed on it.

In the synthesize mode the output exhibits phase jitter for 10Hz reference frequency and low values of N selected. This jitter could be reduced by increasing the low pass filter capacitor but this would mean the PLL would take an unacceptable time to lock.

Appendix

To convert the 5-volt peak-to-peak signals to the 10 volt peak-to-peak required by the phase lock loop and divide ICs the interface circuit[3] shown below was used.



The minimum I_B required for transistor saturation is

$$I_B(\text{min}) = I_c/h_{fe} \ .$$

Assuming values of V_{BE} sat = 0.8V and V_{CE} sat = 0.2V then for transistor in saturation

$$I_c = \frac{10 - 0.2}{R_2} = \frac{9.8}{R_2}$$

letting

$$R_2 = 2.2\text{K}$$

$$I_c = \frac{9.8}{2.2}\ \text{mA} = 4.45\text{mA} \ .$$

Assuming h_{fe}(typical) = 100 for a BC108

then

$$I_{B(\text{min})} = 44.5\mu\text{A}$$

$$I_B = \frac{V_{in} - 0.8}{R_1} \ .$$

For TTL a logic '1' is 5 volts,

so for

$$V_m = 5V, \quad I_B = 4.2/R_1 .$$

Now

$$I_B > I_{B(min)} = 4.45\mu A .$$

Therefore

$$\frac{4.2}{R_1} > 4.45\mu A$$

$$R_1 < 94k\Omega ,$$

let

$$R_1 = 82k\Omega .$$

The circuit was found to require a 'speed-up' capacitor, C_s, across R_1 to reduce the transistor turn on time which would otherwise be noticeable on the output waveform at the higher frequencies. A 120pF capacitor was found experimentally to give the required output waveform.

SYMBOLS

A	CD4052 multiplexer address code input
A_{out}	CD4052 multiplexer channel A output
A_X	CD4052 multiplexer channel A input X
A_Y	CD4052 multiplexer channel A input Y
B	CD4052 multiplexer address code input
B_{in}	CD4052 multiplexer channel B input
B_X	CD4052 multiplexer channel B output X
B_Y	CD4052 multiplexer channel B output Y
C	low pass filter capacitor
C_{out}	CD4052 multiplexer channel C output
C_T	VCO frequency range timing capacitor
C_X	CD4052 multiplexer channel C input X
C_Y	CD4052 multiplexer channel C input Y
f_c	PLL frequency capture range
f_{IN}	programmable divide-by-N counter input signal's frequency
f_L	PLL frequency lock range
f_0	PLL free running frequency
IC	integrated circuit
PLL	phase lock loop
R_A	low pass filter series resistor
R_B	low pass filter parallel resistor
R_0	VCO frequency range offset resistor
R_T	VCO frequency range tuning resistor
TTL	transistor-transistor logic
V_C	VCO control signal
V_d	phase comparator output error signal
V_I	phase comparator input signal
V_0	VCO output signal
VCO	voltage controlled oscillator

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No.	Author	Title, etc.
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2	V. Uzunoglu	*Analysis and design of digital systems.* Gordon and Breach Science Publishers (1975)
3	J. Millman C.C. Halkias	*Integrated electronics.* International student edition, p.165. McGraw-Hill, Kogakusha Ltd. (1972)
4	RCA	*COS-MOS integrated circuits.* 1975 data book series, p.232, RCA Solid state
5	RCA	*COS-MOS integrated circuits.* 1975 data book series, pp.285-286, RCA Solid state

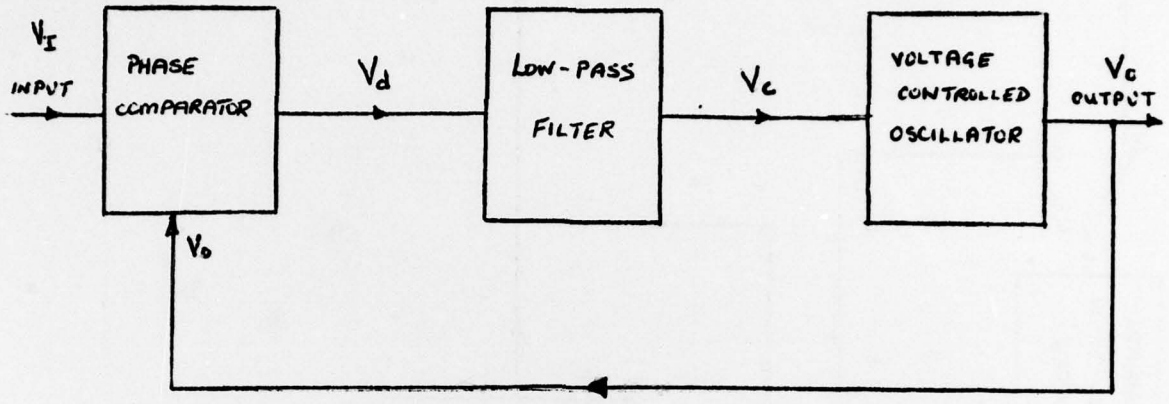

Fig.1 Phase lock loop basic block diagram

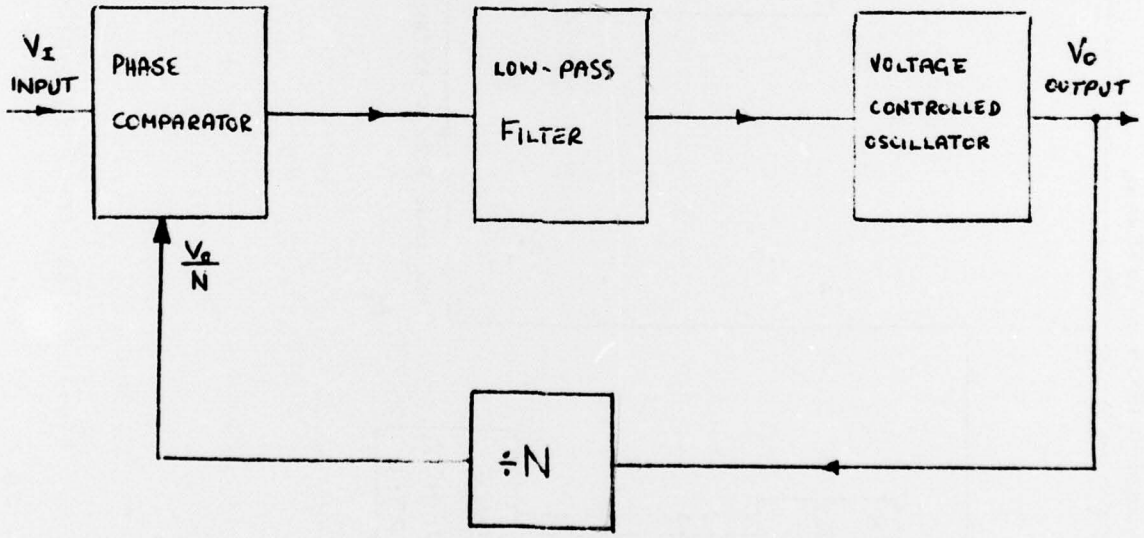

Fig.2 Phase lock loop used as a frequency synthesiser

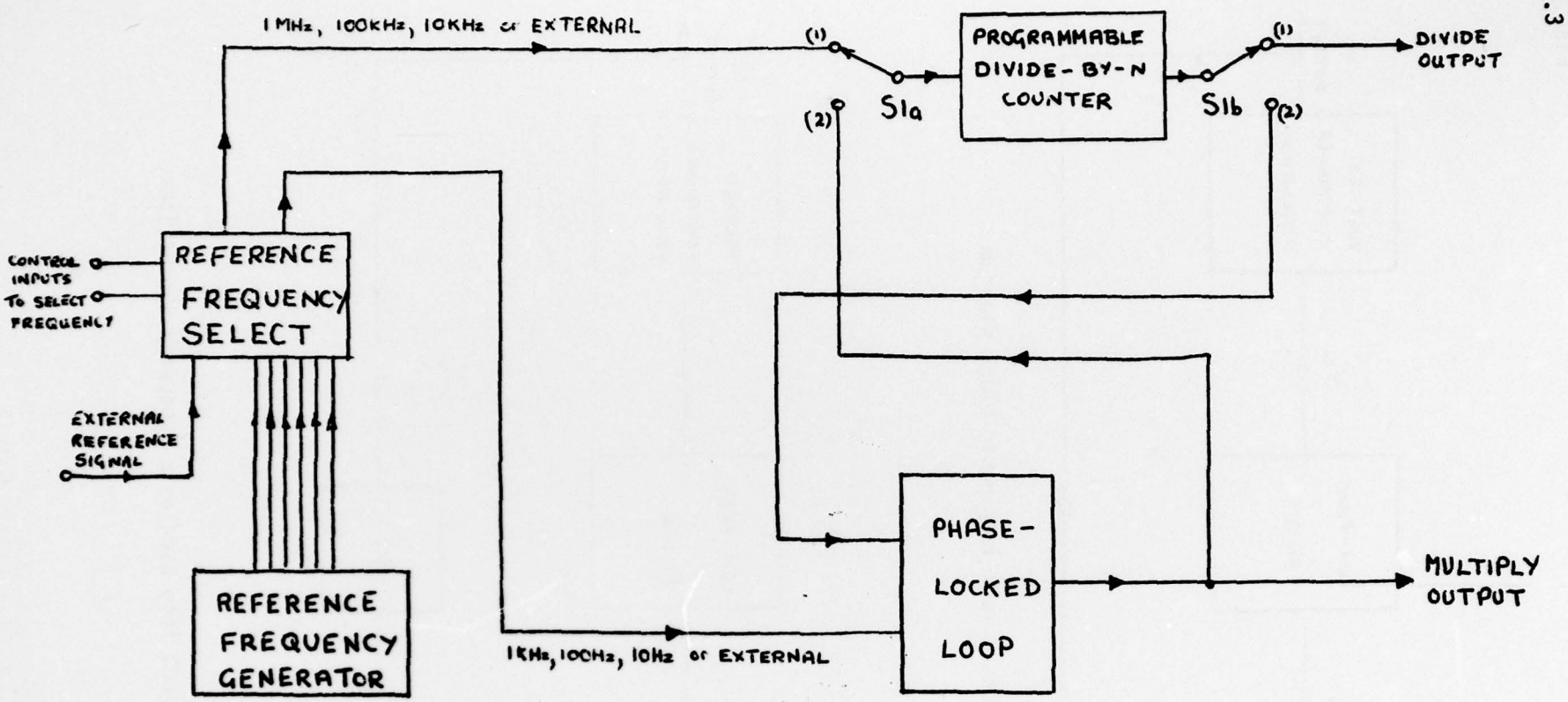

Fig.3

Fig.3 Digital frequency synthesizer/divider

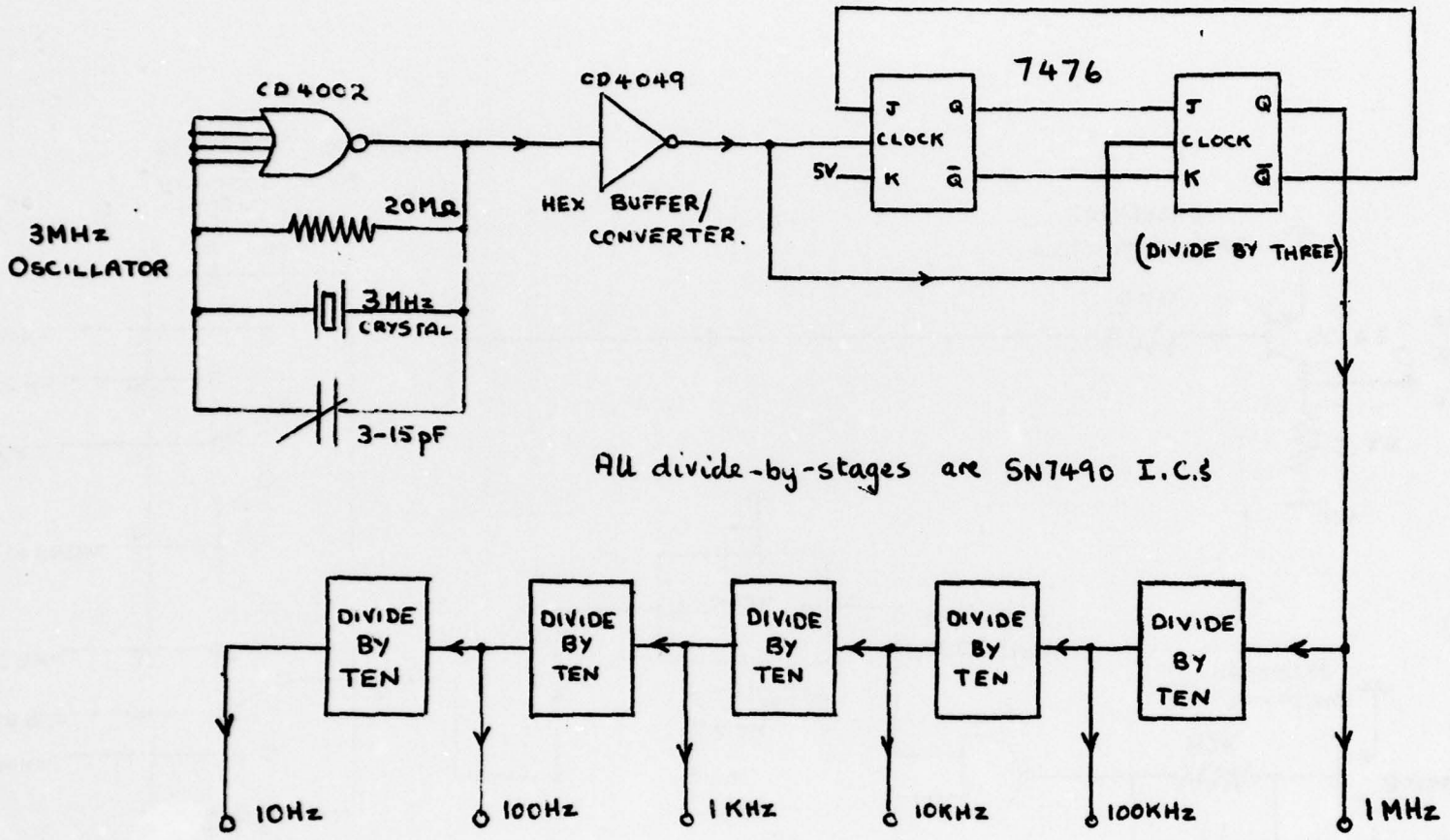

Fig.4 3MHz oscillator and divider chain for internal reference frequencies

Fig.4

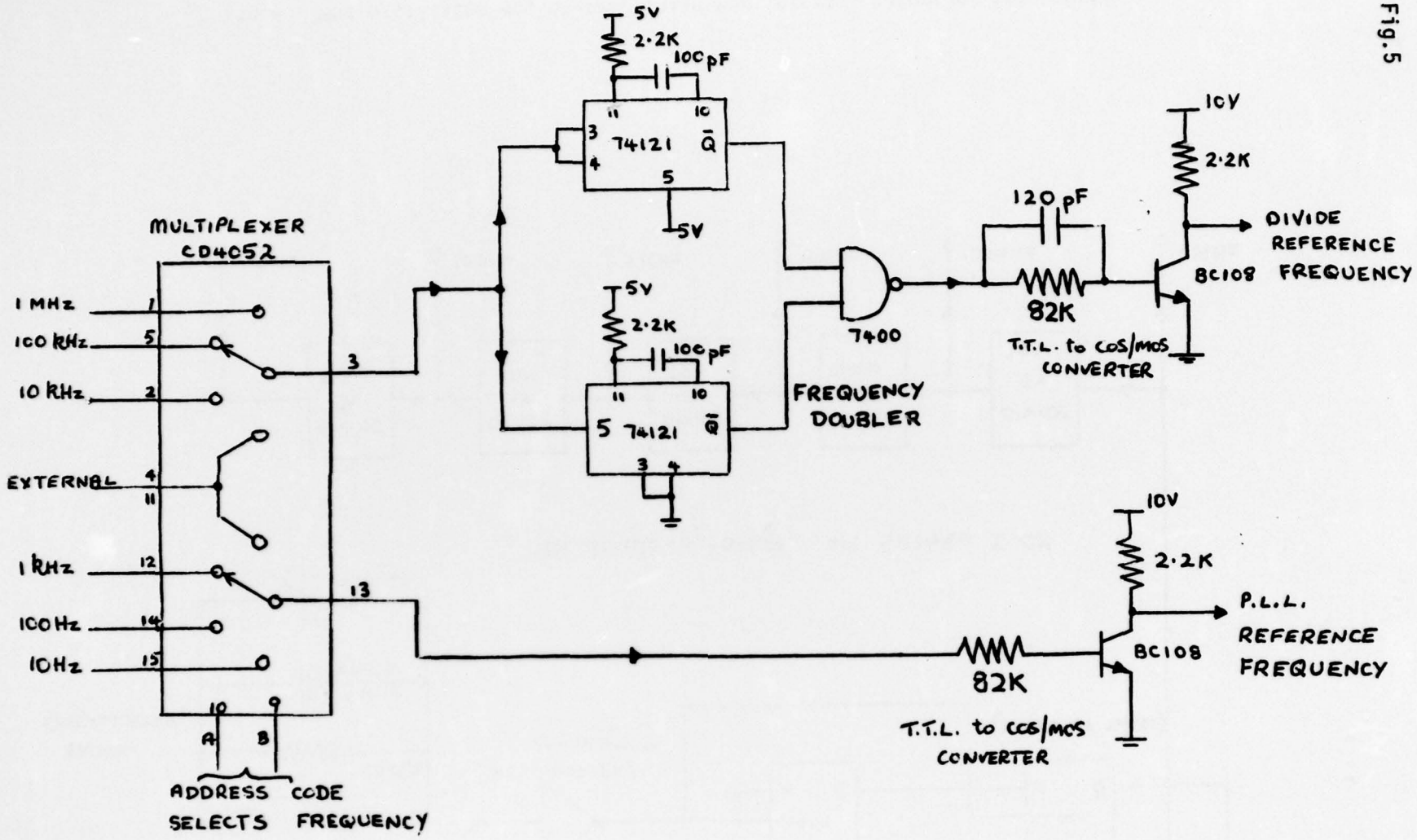

Fig.5

Fig.5 PLL and divide, reference frequency selection

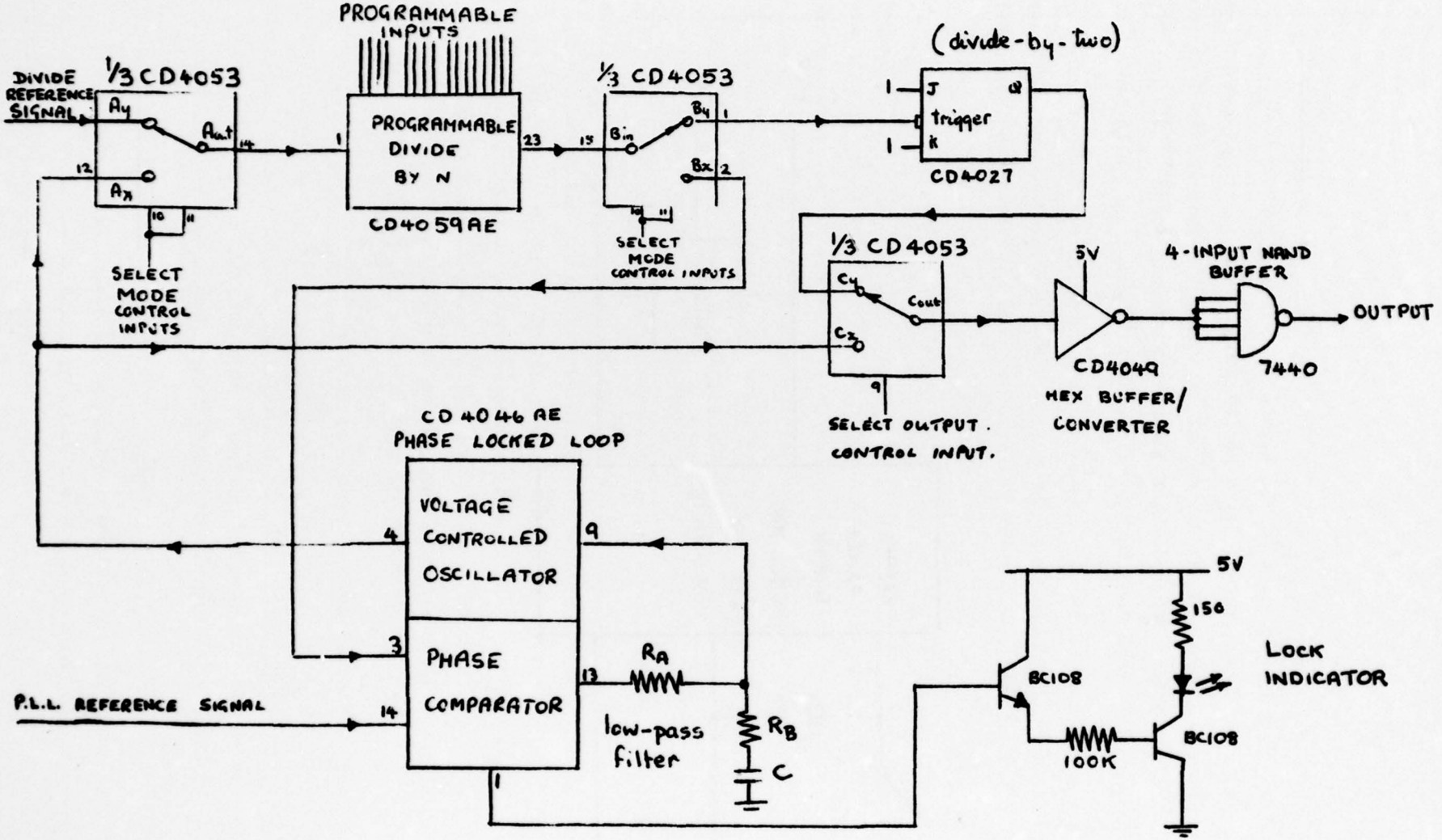

Fig.6 Phase locked loop and divide circuitry

Fig.6

Fig.7

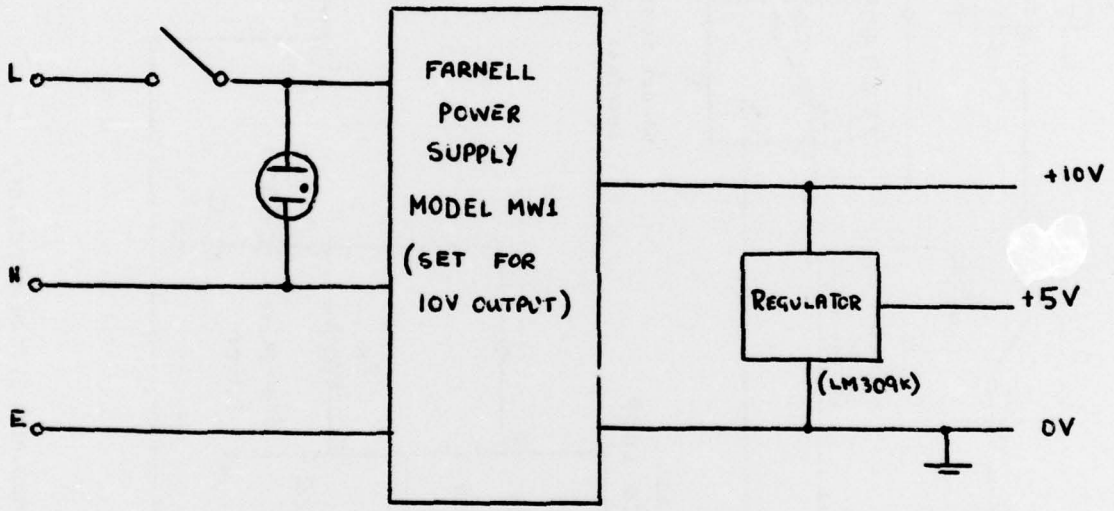

Fig.7 Power supplies

REPORT DOCUMENTATION PAGE

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1. DRIC Reference (to be added by DRIC)	2. Originator's Reference	3. Agency Reference	4. Report Security Classification/Marking
	RAE TM Rad-Nav 43	N/A	UNCLASSIFIED

5. DRIC Code for Originator	6. Originator (Corporate Author) Name and Location
850100	Royal Aircraft Establishment, Farnborough, Hants, UK
5a. Sponsoring Agency's Code	6a. Sponsoring Agency (Contract Authority) Name and Location
N/A	N/A

7. Title: A digital frequency synthesizer-divider using a phase lock loop control system

7a. (For Translations) Title in Foreign Language

7b. (For Conference Papers) Title, Place and Date of Conference

8. Author 1. Surname, Initials	9a. Author 2	9b. Authors 3, 4	10. Date	Pages	Refs.
Lillie, J.			October 1976	18	5

11. Contract Number	12. Period	13. Project	14. Other Reference Nos.
N/A	N/A		

15. Distribution statement
(a) Controlled by – Head of Radio and Navigation Dept.
(b) Special limitations (if any) –

16. Descriptors (Keywords) (Descriptors marked * are selected from TEST)

Phase lock loop. Frequency synthesizer.

17. Abstract

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